

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yasuyoshi ITOH, et al.

SERIAL NO: New Application

GAU:

FILED: Herewith

EXAMINER:

FOR: SEMICONDUCTOR DEVICE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

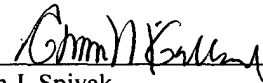
- ☐ Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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STATEMENT OF RELEVANCY

Reference AO (2000-260887) of Form PTO-1449:

“Non-Volatile Semiconductor Memory Device and Manufacturing Method Thereof”

Fig. 2 shows a semiconductor device according to this reference. In the semiconductor device shown in Fig. 2, a stripe-shaped trench 8 is provided between a source region 3s and a drain region 3d formed on a semiconductor substrate 1. A tunnel insulating film 9 is provided on an inner face of the trench 8. A floating gate 33 is buried in the trench 8 via the tunnel insulating film 9. Further, a control gate 35 is provided on the floating gate 33 via an insulating film 34. In operation, a channel region is formed along a periphery of the trench 8.

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 239339US2		SERIAL NO. New Application	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Yasuyoshi ITOH, et al.			
				FILING DATE Herewith		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	5,768,192	06/16/98	Boaz EITAN			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO	2000-260887	09/22/00	Japan		X	✓
	AP	5-75133	03/26/93	Japan (with English extract)		X	✓
	AQ	2002-26149	01/25/02	Japan (with partial English translation)		X	✓
	AR						
	AS						
	AT						
	AU						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AV	Ilan BLOOM, et al., "NROM™ – A NEW NON-VOLATILE MEMORY TECHNOLOGY: FROM DEVICE TO PRODUCTS", Microelectronic Engineering 59, 2001, pgs. 213 – 223. ✓					
	AW	Toshiyuki TOYOSHIMA, et al., "0.1μm LEVEL CONTACT HOLE PATTERN FORMATION WITH KrF LITHOGRAPHY BY RESOLUTION ENHANCEMENT LITHOGRAPHY ASSISTED BY CHEMICAL SHRINK (RELACS)", IEEE, IEDM, 1998, pgs. 333 – 336. ✓					
	AX	J. De BLAUWE, et al., "Si-Dot NON-VOLATILE MEMORY DEVICE", Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pgs. 518 – 519. ✓					
	AY	Boaz EITAN, et al., "CAN NROM, A 2-BIT, TRAPPING STORAGE NVM CELL, GIVE A REAL CHALLENGE TO FLOATING GATE CELLS?", Presented at the International Conference on Solid State Devices and Materials, Tokyo, 1999, pgs. 1/3 – 3/3. ✓					
	AZ	Eli LUSKY, et al., "ELECTRON DISCHARGE MODEL OF LOCALLY-TRAPPED CHARGE IN OXIDE-NITRIDE-OXIDE (ONO) GATES FOR NROM™ NON-VOLATILE SEMICONDUCTOR MEMORY DEVICES", Presented at the Solid State Device and Materials Conference (SSDM 2001), Sep. 2001, Tokyo, Japan, pgs. 1 – 2.				<input type="checkbox"/> Additional References sheet(s) attached <div style="text-align: right;">✓</div>	
Examiner					Date Considered		
<small>*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>							